Catalyst 9300
Switching Architecture

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BRKARC-3863
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A New Era of Networking

Previous Era

Video
Voice
Data

New Era

Security
Cloud
IOT
Mobility
Is Your Network Ready for the New Era?

Does the platform support new PoE devices efficiently?

Does the platform make it easy to provision and scale?

Does the platform support enough Programmability?

Does the platform ensure secure network access?

Does the platform let you adapt to new connectivity requirements?
New Era of Networking – Catalyst 9300

- Integrated security
  - Network as a Sensor
  - Encrypted Traffic Analytics
  - Macsec Encryption
  - Trustworthy Systems

- Mobility ready
  - Fabric Enabled Wireless
  - Unified control and policy

- IoT ready
  - CoAP
  - POE Enhancements
  - IEEE 1588

- Cloud ready
  - Devops Toolkit
  - Streaming Telemetry
  - SDA
  - Web UI
  - Patchability
  - GIR
“The goal of this session is to give you an in depth view of the platform so you can understand its strength as well as its limitations …”
Agenda

• Introduction & Overview
• Platform Architecture, ASIC & Packet Walks
• Stacking Architecture & High Availability
• Differentiating Features & IOS-XE
• Wrap up
Hardware Innovations
Introducing Catalyst 9300
New Generation of Fixed Access

The Next Level of the Market-Leading Fixed Access Switching Platform
Industry’s First High Density Multigigabit Switch
New Generation of Fixed Access

24 Multigigabit Ethernet ports (10G, 5G, 2.5G, 1G)
Cisco UPOE® on all ports
Line rate on all ports

The Next Level of the Market-Leading Fixed Access Switching Platform
Uplink Options on Catalyst 9300

- 4x1Gig SFP
- 8x10Gig SFP/SFP+
- 2x40Gig QSFP
- 4x1/2.5/5/10Gig Copper

Uplink modules supported on all 9300 Series copper models

Online Insertion and Removal (OIR) supported on all uplink modules
Power supplies

Cisco® Catalyst® 9300 Series

- 350W AC
- 750W* DC
- 715W AC
- 1100W AC

Same as 3850—interchangeable new product IDs

Stack cables

Cisco Catalyst 9300 Series

- 3 lengths of cable: 0.5, 1, and 3 meters
- 3 rings
Catalyst 9K Family – Optional Bluetooth

Accessing the Device has never been Easier

cat9k (config)# interface bt0
Catalyst 9K Family – External Storage Options

For Local Logging – 3rd Party App Hosting - Containers

USB 2.0/3.0*

Up to 120 GB
Catalyst 9300 – Blue Beacon

Blue Beacon on Every System

Identification of Devices has never been Easier
Sample RFID Tag Data

- **SN** = 'FOC2109Q023'
- **PID** = 'C9300-24P'
- **VID** = 'V00'
- **TAN** = '68-100900-02'
- **TAN Rev** = '10'
- **CLEI** = 'UNDEFINED'
- **Index** = '900'
- **Encode** = 'SGTIN-198'
- **Filter** = '0'
- **Partition** = '5'

Inventory Management (Tracking) has never been Easier
High Availability – Stackwise-480

Centralized Control Plane

Distributed Data Plane

Up to 8 Members

1+1 Stateful Redundancy with Active & Standby

Stateful Switchover SSO/NSF

Stackwise-480
StackPower - Overview

“Zero-Footprint” RPS deployment

- Provides RPS functionality with Zero RPS Footprint
- Pay-as-you-grow architecture – similar to the Data Stack
- 1+N Redundancy with Inline Power
- Up to 4 Switches in a StackPower Ring
- Multiple StackPower Possible within one Data Stack
- Up to 9 Switches in a star topology with XPS
The New Catalyst 9300

- Unmatched POE
  - Resiliency – Perpetual/Fast
  - High power - 60W UPOE

- In-Built Memory
  - 8GB Memory
  - 16GB Flash

- Powerful CPU complex
  - X86 CPU
  - 4-core 1.8GHz

- Flexible ASIC
  - UADP 2.0

- Most Dense and Flexible Uplink offering
  - 8x10G, 4 x MGig, 2 x 40G

- Built-in RFID
  - Passive

- Bluetooth Dongle Support/External Storage
  - (USB 2.0)

- In-Built Memory

- USB Console
  - Mini-USB type B

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Catalyst 9300—Back View

- **External Storage**: USB 3.0 Removable storage (120GB SSD)
- **Stackwise-480**: 8 members NSF/SSO
- **Stack Cables**
- **Redundant Fans**
- **Redundant Power Supply**
- **Optional PS Power Supplies (AC+DC*)**

*Roadmap*
Looking Inside the Switch
Catalyst 9300: Under the Covers…
Catalyst 9300: Under the Covers…
Catalyst 9K Family - x86 CPU

x86 CPU enables hosting containers and 3rd party apps
ASICs are a Pillar of Cisco Innovation...
Traditional Networking ASICs - Fixed Pipelines

- MAC Look up
- IPv4 Look up
- ACL Look up
- QoS Look up

Not Supported in Hardware

Fixed Pipeline
New ASICs for New Technology?

Marketing Requirements → Architecture → RTL Design → Synthesis → Floor Planning → Fabrication

2 – 4 Years

Building a new ASIC takes a lot of time & money
How about CPUs?

CPUs are highly programmable.

CPUs are not as fast.
Traditional Networking ASICs vs CPUs

Performance
Flexibility

Performance
Flexibility

Traditional Networking ASIC

General Purpose CPU

Purpose Built – High Performance

General Purpose – Highly Flexible
In 2013 Cisco Introduced UADP (Unified Access Data Plane)

UADP brings Flexibility without compromise on Performance
UADP Evolution

UADP 1.0
1.6 Billion Transistors
36 nm

UADP 1.1
3.2 Billion Transistors
36 nm

Catalyst 3850 Copper
Catalyst 3650
Catalyst SFP Fiber
Catalyst 3850 Multigigabit
Catalyst 3850 SFP+
Catalyst 3650 Mini
Catalyst 3650 Multigigabit
UADP 2.0 - Next Generation of ASIC Innovation

- Investment Protection
  - Flexible Pipeline
- Universal Deployments
  - Adaptable Tables
- Enhanced Scale/Buffering
  - Multicore resource share

- 384K Flex Counters
- Shared Lookup
- Up to 240GE Bandwidth
- Up to 2X to 4X Forwarding + TCAM

- Embedded Microcontrollers
- Up to 32MB Packet Buffer
- Up to 64K x2 Netflow Records

- 7.46B Transistors
- 28nm Technology
Some of the Key Capabilities of UADP 2.0

Flex Parser & Programmable Pipelines

Recirculation Capability

Micro Engines

Adaptable Tables

No Compromise on Performance
UADP 2.0 – Core Architecture

Stack Interface

PBC – Packet Buffers Complex

Ingress Forwarding Controller (IFC)

Flexible Look up Tables (Shared Across Cores)

Egress Forwarding Controller (EFC)

Encryption Engine

Recirculation Engine

ReWrite Engine

Network Interfaces - Front Panel Ports + CPU + Network Redundant Uplinks (NRU)
UADP 2.0 – Programmable Pipelines
Programmable Pipelines – Closer Look…

- Final Decision on Packet’s Future
- 15 Ingress Programmable Stages
- Flex Parser 256 B
- At each stage, 2 simultaneous lookups
- 8 Egress Programmable Stages
- Flex Parser 256 B
- Final Decision on Packet’s Future

Flexible Look up Tables
(Shared Across Cores)

15 Ingress Programmable Stages

8 Egress Programmable Stages

Flex Parser

256 B
Microcode programs the Pipelines

Programmed to understand VXLAN

Flexible Look up Tables
(Shared Across Cores)

Programmed to understand MPLS

Ingress Programmable Pipeline

Flexible Look up Tables (Shared Across Cores)

Egress Programmable Pipeline
Catalyst 9K

UADP 2.0 Performance – 500 MHz Clock Speed

- 64 B Line Rate (80 Gbps)
- 114Mpps Switching Capacity
- ?? Gbps Streaming Capacity
- Minimal added latency with Recirculation (1/2 us)

- Downlinks + Uplinks 68G
- Recirculation 10G
- CPU 2G

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Platform Architecture & Layouts
Catalyst 9300 —24Port Layout

480G STACK INTERFACE

- Packet Buffer
- Forwarding Controller
- Ingress FIFO
- Egress FIFO
- Reassembly
- Crypto
- Network Interface
- Octal PHY
- 12 Port PoE+
- 24 x 1G 10/100/1000
- 40G PHY
- 4 X 1G, 4 X Mgig, 8 X 10G, 2 X 40G
- MGMT
- Console
- FPGA
- SDRAM 8GB
- Flash 16GB
- USB 2.0
- USB 3.0

- UADP 2.0 ASIC
- Clock - 500 MHz / 160Gbps
- X86 1.8 GHz
- Quad-Core CPU

- ASIC1
- Core 0
- Core 1
- BRKARC - 3863
Catalyst 9300 MultiGigabit — 24 Port Layout

480G STACK INTERFACE

- Packet Buffer
- Forwarding Controller
- Ingress FIFO
- Egress FIFO
- Network Interface
- Reassembly Crypto
- FPGA
- SDRAM
- 8GB
- Flash
- 16GB
- USB 2.0
- USB 3.0
- MGMT
- Console
- 40G PHY
- 40G PHY
- 4 x 1G, 4 x Mgig, 8 x 10G, 2 x 40G
- 12 x 10G 100M/1G/2.5G/5G/10G
- 12 x 10G 100M/1G/2.5G/5G/10G
- 12 Port UPoE
- 12 Port UPoE
- MGig Quad PHY
- MGig Quad PHY
- MGig Quad PHY
- MGig Quad PHY
- X86 1.8 GHz Quad-Core CPU
- UADP 2.0 ASIC Clock – 500 MHz / 160Gbps

Core 0

Core 1

Core 0

Core 1

ASIC0

ASIC1

MGig Quad PHY
MGig Quad PHY
MGig Quad PHY
MGig Quad PHY

12 Port UPoE

12 Port UPoE

12 x 10G 100M/1G/2.5G/5G/10G

12 x 10G 100M/1G/2.5G/5G/10G
ASIC to port Mapping 9300-48P

### 9300-Multigigabit48#show platform software fed switch 1 ifm mappings

<table>
<thead>
<tr>
<th>Interface</th>
<th>IF_ID</th>
<th>Inst</th>
<th>Asic Core</th>
<th>Port</th>
<th>Type</th>
<th>Active</th>
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<tbody>
<tr>
<td>GigabitEthernet1/0/1</td>
<td>0x7</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<td>NIF Y</td>
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<tr>
<td>GigabitEthernet1/0/24</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>23</td>
<td>NIF Y</td>
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<tr>
<td>GigabitEthernet1/0/25</td>
<td>0x1f</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>24</td>
<td>NIF Y</td>
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<tr>
<td>GigabitEthernet1/0/48</td>
<td>0x36</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>47</td>
<td>NIF Y</td>
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<tr>
<td>GigabitEthernet1/1/1</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>48</td>
<td>NIF Y</td>
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<td>51</td>
<td>NIF Y</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>52</td>
<td>NIF Y</td>
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<tr>
<td>TenGigabitEthernet1/1/4</td>
<td>0x3e</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>55</td>
<td>NIF Y</td>
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<td>TenGigabitEthernet1/1/5</td>
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<td>0</td>
<td>0</td>
<td>56</td>
<td>NIF Y</td>
</tr>
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---

**Catalyst 9300-48**

<table>
<thead>
<tr>
<th>Switch Ports Model</th>
<th>SW Version</th>
<th>SW Image</th>
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<tbody>
<tr>
<td>*</td>
<td>1 62</td>
<td>C9300-48P 16.5.1</td>
</tr>
<tr>
<td>CAT9K_IOSXE</td>
<td></td>
<td></td>
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</table>
## Number of ASICs in different versions of Switches

<table>
<thead>
<tr>
<th>Product Version</th>
<th>Number of ASICs/Cores</th>
<th>Clock Speed</th>
<th>Total Bandwidth Available</th>
</tr>
</thead>
<tbody>
<tr>
<td>24/48 Port 9300</td>
<td>1/2</td>
<td>500 MHz</td>
<td>160 G</td>
</tr>
<tr>
<td>24 Port mGig versions</td>
<td>2/4</td>
<td>500 MHz</td>
<td>320G</td>
</tr>
</tbody>
</table>
Packet Walks
Unicast – within ASIC

1. Received, processed by MACSec and into FIFO
2. A copy to buffer and a copy to IFC
3. Goes through IFC, result descriptor send to PBC
4. Descriptor has local destination, PBC sends the info to EQS

1. Ingress Forwarding Controller (IFC)
2. Flexible Look up Tables (Shared Across Cores)
3. Egress Forwarding Controller (EFC)
4. PBC – Packet Buffers Complex
5. SQS, AQM
6. EQS
7. ReWrite Engine
8. Egress FIFO

MACSEC
Network Interfaces - Front Panel Ports + CPU + Network Redundant Uplinks (NRU)
Unic peace – Across ASICs on Input

Stage #8

Flex Parser

Ingress Pipeline

Stage #7

Stage #6

Stage #5

Stage #4

Stage #3

Stage #2

Stage #1

Network Interfaces - Front Panel Ports + CPU + Network Redundant Uplinks (NRU)

MACSEC

Recirculation Engine

Encryption Engine

ReWrite Engine

PBC – Packet Buffers Complex

Egress Forwarding Controller (EFC)

Flexible Look up Tables (Shared Across Cores)

Ingress Forwarding Controller (IFC)

Stack Interface

1. Received, processed by MACSec and into FIFO
2. A copy to buffer and a copy to IFC
3. Goes through IFC, result descriptor send to PBC
4. Descriptor has remote destination, PBC sends the info to IQS
5. IQS schedule PBC to send the packet with descriptor to Stack Interface

SQS AQM

Egress FIFO

PBC – Packet Buffers Complex

Ingress FIFO

ReWrite Engine

Egress Forwarding Controller (EFC)

Flexible Look up Tables (Shared Across Cores)

Ingress Forwarding Controller (IFC)

EQS

ReWrite Engine

Egress Forwarding Controller (EFC)

Flexible Look up Tables (Shared Across Cores)

Ingress Forwarding Controller (IFC)
Unic和平 - Across AS中Ss on Output

Stack Interface

PBC – Packet Buffers Complex

Ingress Forwarding Controller (IFC)

Flexible Look up Tables (Shared Across Cores)

Egress Forwarding Controller (EFC)

Encryption Engine

Recirculation Engine

Network Interfaces - Front Panel Ports + CPU + Network Redundant Uplinks (NRU)

MACSEC

PBC received the frame and sends the info to EQS

6. EQS schedule PBC to send a copy to EFC and a copy to ReWrite (includes descriptor)

7. EFC sends results to ReWrite

8. Rewrite the packet and send it out though the egress FIFO

9. PBC received the frame and sends the info to EQS
Multicast – Egress Local

1. Received, processed by MACSec and into FIFO
2. A copy to buffer and a copy to IFC
3. Goes through IFC, result descriptor send to PBC
4. Descriptor has local destination, PBC sends the info to EQS

1. Ingress Forwarding Controller (IFC)
2. Encryption Engine
3. Recirculation Engine
4. Only a single copy of packet in buffer memory during repliaction
5. AQM within EOS generate the list of egress port based on descriptor, schedule for each egress port
6. For each egress port, frame goes through the EFC, ReWrit and Egress FIFO

Network Interfaces - Front Panel Ports + CPU + Network Redundant Uplinks (NRU)
Multicast – Egress Remote on Input

1. Received, processed by MACSec and into FIFO
2. A copy to buffer and a copy to IFC
3. Goes through IFC, result descriptor send to PBC
4. Descriptor has remote destination, PBC sends the info to IQS
5. IQS schedule PBC to send the packet with descriptor to Stack Interface

Descriptor can contains both local and remote destinations
Multicast – Egress Remote Output

Stack Interface

PBC – Packet Buffers Complex

Ingress Forwarding Controller (IFC)

Flexible Look up Tables (Shared Across Cores)

Egress Forwarding Controller (EFC)

Encryption Engine

Recirculation Engine

Ingress FIFO

Egress FIFO

MACSEC

Network Interfaces - Front Panel Ports + CPU + Network Redundant Uplinks (NRU)

Replication done on egress => Efficient use of BW

6. PBC received the frame and sends the info to EQS
7. AQM within EQS generate the list of egress port based on descriptor, schedule for each egress port
8. For each egress port, frame goes though the EFC, ReWrite and Egress FIFO

Replication done on egress => Efficient use of BW

6. PBC received the frame and sends the info to EQS
7. AQM within EQS generate the list of egress port based on descriptor, schedule for each egress port
8. For each egress port, frame goes though the EFC, ReWrite and Egress FIFO
Forwarding and TCAM Resources
Flex Tables

- SRAM: Lookup Table
- TCAM: Lookup Table

Diagram showing multiple Lookup Tables in SRAM and TCAM sections.
ASIC Lookup Tables

Forwarding Resources

TCAM Resources

Netflow
Lookup Tables

**Forwarding Resources**
- MAC
- Host Route
- IGMP Groups
- LPM Route
- Multicast Route
- SGT

**TCAM Resources**
- Security ACL
- QoS ACL
- Service ACL
  - PBR
  - Netflow ACL
  - SPAN
  - MACsec
  - CoPP
  - Tunnel
  - LISP

**Netflow**

**Netflow Entries**
Lookup Tables

Forwarding Resources

- MAC: 32K
- Host Route: 24k
- IGMP Groups: 8k
- LPM Route: 8k
- Multicast Route: 8k
- SGT: 8k

Feature Resources

- Security ACL: 5k
- QoS ACL: 5k
- Service ACL: 4k
  - PBR
  - Netflow ACL
  - SPAN
  - MACsec
  - CoPP
  - Tunnel
  - LISP

Netflow

Netflow Entries: 64k per ASIC
Scale and TCAM Partition

- Each IPv6 ACL (without port range) requires two TCAM entries.

```
CAT9K#show platform hardware fed switch active fwd-asic resource tcam utilization 0
CAM Utilization for ASIC Instance [0]

<table>
<thead>
<tr>
<th>Table</th>
<th>Max Values</th>
<th>Used Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unicast MAC addresses</td>
<td>32768/512</td>
<td>16/22</td>
</tr>
<tr>
<td>IGMP and Multicast groups</td>
<td>8192/512</td>
<td>0/0</td>
</tr>
<tr>
<td>L2 Multicast groups</td>
<td>8192/512</td>
<td>0/0</td>
</tr>
<tr>
<td>Directly or indirectly connected routes</td>
<td>24576/8192</td>
<td>10/21</td>
</tr>
<tr>
<td>NAT/PAT SA address and Port</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>QoS Access Control Entries</td>
<td>5120</td>
<td>0</td>
</tr>
<tr>
<td>Security Access Control Entries</td>
<td>5120</td>
<td>126</td>
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<tr>
<td>Ingress Netflow ACEs</td>
<td>256</td>
<td>9</td>
</tr>
<tr>
<td>Policy Based Routing ACEs</td>
<td>1024</td>
<td>0</td>
</tr>
<tr>
<td>Egress Netflow ACEs</td>
<td>768</td>
<td>0</td>
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<tr>
<td>Input Microflow policer ACEs</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Output Microflow policer ACEs</td>
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<td>0</td>
</tr>
<tr>
<td>Flow SPAN ACEs</td>
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<tr>
<td>Control Plane Entries</td>
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<td>204</td>
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<tr>
<td>Tunnels</td>
<td>512</td>
<td>17</td>
</tr>
<tr>
<td>Lisp Instance Mapping Entries</td>
<td>512</td>
<td>3</td>
</tr>
<tr>
<td>Input Security Associations</td>
<td>256</td>
<td>0</td>
</tr>
<tr>
<td>Output Security Associations and Policies</td>
<td>256</td>
<td>0</td>
</tr>
<tr>
<td>SGT_DGT</td>
<td>8192/512</td>
<td>0/1</td>
</tr>
<tr>
<td>CLIENT_LE</td>
<td>4096/256</td>
<td>0/0</td>
</tr>
<tr>
<td>INPUT_GROUP_LE</td>
<td>1024</td>
<td>0</td>
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<tr>
<td>OUTPUT_GROUP_LE</td>
<td>1024</td>
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</tr>
<tr>
<td>Macsec SPD</td>
<td>256</td>
<td>2</td>
</tr>
</tbody>
</table>
```
Dafault SDM Template

Network Interface

Forwarding
- FIB (8k)
- Host (16k)
- MCAST (8k)
- IGMP (8k)
- SGT (8K)
- MAC (32k)
- Internal Resources

TCAM
- SEC ACL (5k)
- QoS ACL (5k)
- Tunnels (512)
- LISP (512)
- Others
- Internal Resources

Packet Buffer

Netflow

Stack Interface
Stacking Architecture
The Stack Ring

480 Gbps capacity

6 Rings in the Stack

- 6 rings in total
- 3 rings go East
- 3 rings go West
- Each ring is 40Gbps
- 240Gbps uni-direction
- Spatial Reuse= 480Gbps

Assuming 4 x 24-port 9300 Switches
Unicast Packet Path on the Stack Ring

Assuming 4 x 24-port 9300 Switches

- Packet segmented into 256 bytes
- Packet travels half the ring for unicast traffic
- Segments reordered at destination stack port
- Destination strips the packet off the stack ring
Stack Ring Spatial Reuse

Assuming 4 x 24-port 9300 Switches

- Credit based system on the Stack Ring
- Multiple stack ports grab the ring that is free and they have credits on to transmit
- Increases the stack ring bandwidth to 480Gbps
Multicast Packet Path on Stack Ring

Assuming 4 x 24-port 9300 Switches

- One copy of the source packet is placed on the rings
- Interested Stack Ports grab the segments when they see them
- Packet segments travel the whole ring back to source
- The source strips these segments off the ring (Source Stripping)
- Results in efficient replication of multicast traffic for multiple Stack Port receivers
High Availability
Stacking Architecture

480G STACK INTERFACE

- **Packet Buffer**
- **Forwarding Controller**
- **Ingress FIFO**
- **Egress FIFO**
- **Network Interface**

**ASIC1**
- **Core 1**
- **Core 0**

**ASIC0**
- **Core 1**
- **Core 0**

- **MGig Quad PHY**
- **12 Port UPoE**
- **12 x 10G 100M/1G/2.5G/5G/10G**

- **40G PHY**
- **4X1G, 4X Mgig, 8X10G, 2X40G**

- **UADP 2.0 ASIC**
  - **Clock**: 500 MHz / 160 Gbps

- **X86**
  - **1.8 GHz Quad-Core CPU**

- **FPGA**
- **SDRAM**
  - **8GB**
- **Flash**
  - **16GB**

- **USB 2.0**
- **USB 3.0**

- **Console**

- **MGMT**

**Notes:**
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Stackwise-480 Architecture

Centralized Control Plane – Scalable Distributed Data Plane
How many Can I stack together?

- Up to 8 Switches can be stacked together using back stacking cables
- All 9300 models are supported in the stack
- All the switches in the stack should run the same IOS and License
Stack Discovery

- Stack Interfaces brought online
- Infra and LC Domains boot in parallel
- Stack Discovery Protocol discovers Stack topology – broadcast, followed by neighborcast
- In full ring, discovery exits after all members are found.
- In half ring, system waits for 2mins
- Active Election begins after Discovery exits

Stack port 1 cable is connected and the link is up
Stack port 2 cable is connected and the link is up
Waiting for 120 seconds for other switches to boot
%IOSXE-1-PLATFORM: process stack-mgr: %STACKMGR-1-DISC_START: Switch 3 is starting stack discovery.
##All switches in the stack have been discovered

Switch number is 3
%IOSXE-1-PLATFORM: process stack-mgr: %STACKMGR-1-DISC_DONE: Switch 3 has finished stack discovery.
%IOSXE-1-PLATFORM: process stack-mgr: %STACKMGR-1-SWITCH_ADDED: Switch 3 has been added to the stack.
Stack Active Election

1) The stack (or switch) whose member has the higher user configurable priority 1–15

2) The switch or stack whose member has the lowest MAC address

%IOSXE-1-PLATFORM: process stack-mgr: %STACKMGR-1-ACTIVE_ELECTED: Switch 3 has been elected ACTIVE.
Stack Initialization

- Active starts RP Domain (IOSd, WCM, etc) locally
- Programs hardware on all LC Domains
- Traffic resumes once hardware is programmed
- Starts 2min Timer to elect Standby in parallel
- Active elects Standby
- Standby starts RP Domain locally
- Starts Bulk Sync with Active RP
- Standby reaches “Standby Hot”

%STACKMGR-1-STANDBY_ELECTED: 3 stack-mgr: Switch 2 has been elected STANDBY.

GUIDELINE#show switch
Switch/Stack Mac Address : 2037.0652.a580 - Local Mac Address
Mac persistency wait time: Indefinite

<table>
<thead>
<tr>
<th>Switch#</th>
<th>Role</th>
<th>Mac Address</th>
<th>Priority</th>
<th>Version</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Member</td>
<td>2037.0653.ca80</td>
<td>5</td>
<td>P6A</td>
<td>Ready</td>
</tr>
<tr>
<td>2</td>
<td>Standby</td>
<td>2037.0653.db00</td>
<td>10</td>
<td>P6A</td>
<td>HA sync in progress</td>
</tr>
<tr>
<td>*3</td>
<td>Active</td>
<td>2037.0652.a580</td>
<td>15</td>
<td>V01</td>
<td>Ready</td>
</tr>
</tbody>
</table>
HA Best Practices & Recommendations

- Power up the first Switch that you want to make it as Active
- Configure Priority of the switch (1-15) – 1 by default – the higher the better
- Power up the second member that you want to make as Standby & then power up rest of the members
- To add a member to an existing stack plug in the stack cable first, then power up the switch
- Avoid stack Merge & Stack split if possible

Catalyst9300#switch 1 priority 15
Catalyst9300#switch 2 priority 14
Catalyst9300#switch 3 priority 13
Catalyst9300#switch 4 priority 12
Stack Member Addition

- Stack discovery initiated and completed
- Plug in the member, completing full ring
- Power up the member
- Stack Discovery process runs and completes immediately after discovery happens
- Active detects the new addition, and programs the hardware of the member
- Active is not pre-empted by powering on another member even if it was High Priority
Stack Member Addition – Software Upgrade

- All stack members must have common IOS software version to pair in SSO redundancy state
- Stack member with version mis-match with ACTIVE switch will fail to RPR mode
- Enable “software auto-upgrade enable” command to automate upgrade process
- System must boot in install mode (default and recommended). Auto Upgrade not supported in Bundle Mode
Stack Member Deletion

- Stack discovery initiated and completed
- Active detects member removal – and Clean up process is initiated
- Clean-up involves removing TCAM entries referencing removed member, MAC addresses, CDP tables – more like all ports on the member are shutdown
- Configuration is moved to Pre-Provisioned state
Scale - TCAM, Queues, Memory, ACLs...
Higher and Flexible ACL Scale

Feature Resources

- Security ACL: 5K
- QoS ACL: 5K
- Service ACL: 5K
  - Netflow ACL
  - SPAN
  - MACsec
  - CoPP
  - Tunnel
  - LISP

ACL Resources

| IPv4 Entries | 5000 Entries |
| IPv6 Entries | Half the IPv4 |
| One type of IPv4 ACL (RACL, PACL, VACL, GACL*) | 5000 Entries |
| L4OPs/Label  | 8 L4OPs      |

ACL – Ingress/Egress

- Each ACL policy is referenced by a label. This same label is assigned to multiple interfaces and VLANs

Label1
Netflow on Catalyst 9300

- Flexible Netflow / Full Netflow
- Source IP
- Dest IP
- Source Port
- Dest Port
- L3 Protocol
- Src MAC
- Etc..

Netflow Enabled Device

- 64k/ASIC
- 32k IPv4 Ingress
- 32k IPv4 Egress
- Both Ingress and egress netflow supported simultaneously
- Distributed Forwarding/Export

Netflow Cache

<table>
<thead>
<tr>
<th>Flow Information</th>
<th>Packets</th>
<th>Bytes/Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP,Ports</td>
<td>32000</td>
<td>1100</td>
</tr>
</tbody>
</table>

Export

- X86 1.8 GHZ CPU
- No impact on CPU with default timers

Collector
QoS Fundamental Actions

Trust → Classification → Policing → Conditional Marking

Classification → Unconditional Marking → Policing

Conditional Marking → Policing → Classification

Unconditional Marking → Classification

Scheduler

8q3t
1p7q3t
2p6q3t

PQ1
PQ2
Q3
Q4
Q5
Q6
Q7
Q7
WTD rest of non WRED queues

WRED on any 4 queues

PQ or Q

WTD
## Catalyst 9300—QoS Scalability

<table>
<thead>
<tr>
<th>QoS Scale Numbers</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Class-maps (Ingress)</td>
<td>1024</td>
</tr>
<tr>
<td>Class-maps (egress)</td>
<td>512</td>
</tr>
<tr>
<td>Table-maps (ingress)</td>
<td>16</td>
</tr>
<tr>
<td>Table-maps (egress)</td>
<td>16</td>
</tr>
<tr>
<td>Aggregate Policers</td>
<td>2000</td>
</tr>
<tr>
<td>Microflow Policers</td>
<td>24000</td>
</tr>
<tr>
<td>Queues/port</td>
<td>8 queues</td>
</tr>
<tr>
<td>Buffer/ASIC</td>
<td>16 MB</td>
</tr>
</tbody>
</table>
QOS – Higher Packet Buffer

Packets to Egress Port Queues

- 5 MB AQM
- 1.5 MB SQS
- 1 MB IQS
- 0.5 MB Packet Holding Buffer
- Packets going to Stack
- Packets from the Stack And Locally Switched Packets

Packet Buffer
- 8MB/Core, 16MB/ASIC
- Shared across Ingress and Egress
- IQS and SQS intelligently shared the common-shared,
  - Buffer organized in cells of 256 Bytes each

QOS
- WRED Support Added

Performance
- Line rate across all ports
- Jumbo Frames Support

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Catalyst 9300 Software
IOS XE Evolution
Same Look & Feel, More Powerful Architecture

<table>
<thead>
<tr>
<th>IOS</th>
<th>IOS XE 3.7.x(SE)</th>
<th>IOS XE Denali 16.1.1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Features Components</strong></td>
<td><strong>IOSd</strong> Features Components</td>
<td><strong>IOSd</strong> Features Components</td>
</tr>
<tr>
<td>Common Infrastructure / HA</td>
<td>Hosted Apps WCM Wireshark</td>
<td>Hosted Apps WCM Wireshark</td>
</tr>
<tr>
<td>Management Interface</td>
<td>Module Drivers</td>
<td>Common Infrastructure / HA</td>
</tr>
<tr>
<td>Module Drivers</td>
<td>Kernel</td>
<td>Management Interface</td>
</tr>
<tr>
<td>Kernel</td>
<td></td>
<td>Module Drivers</td>
</tr>
</tbody>
</table>

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IOS-XE 16

- **One Release Train**
  Operational Efficiency, Consistency in Control Plane Behavior,

- **RAFA**
  (Run Any Feature Anywhere)
  Feature Velocity across Platforms

- **Patch Updates**
  WCM/SANET/etc sub package upgrade, Peace of mind for Customers

- **Comprehensive Programmability**
  Object based model, Netconf/REST Interfaces

- **Secure Platform**
  64 Bit ASLR, Mandatory Access Control for Processes
Software-Defined Access
Solution Components

DNA Center: Simple Workflows

Design
Provision
Policy
Assurance

DNA Center

Network Data Platform
APIC-EM
Identity Services Engine

Routers
Switches
Wireless AP
WLC
Catalyst 9300 – Trustworthy Systems

Catalyst 9K Family is Built with Security

- Trustworthy Systems
- Image Signing Authentic OS
- PnP SUDI Support Two Way Trust
- Hardware Authenticity Genuine Hardware
- Runtime Defenses 64 Bit ASLR
- Secure Boot Boot Sequence Check
- Integrity Verifications Malware Protection
- BRKARC-3863
Catalyst 9K Family – Encrypted Traffic Analytics

StealthWatch

Netflow with New Extensions

Catalyst 9K Family

Encrypted Threat Analytics

99%+ Accuracy
Catalyst 9300 – Leadership in PoE Features

- **2-event classification**
  - Fast power negotiation without LLDP
  - Physical layer negotiation < 1 sec

- **Perpetual UPOE**
  - Uninterrupted PoE power during control plane reboot

- **Fast UPOE**
  - Bypasses Cisco IOS® control plane boot
  - Restores power to PD within 30 sec of power resumption
Graceful Insertion and Removal (GIR)

- Hardware replacement
- Software upgrades
- Configuration changes

Gracefully remove or insert a node without impacting traffic

Layer 3
Layer 2

IS-IS, BGP, OSPF
Catalyst 9K enables Real Time Streaming Telemetry

Traditional Networking

Proprietary, Unstructured (MIBs, CLI)

Data Models

Standards-Based, Structured (IETF YANG, OpenConfig)

Data Representation & Export

Fast, Reliable, Flexible, Streaming (NetConf - XML, RestConf – JSON, gRPC)

Raw, L1-L3 Oriented

Locally Enriched, Application Oriented

- Data Models
  - Slow, Error-Prone, Query-based (SNMP)
  - Proprietary, Unstructured (MIBs, CLI)
  - Fast, Reliable, Flexible, Streaming (NetConf - XML, RestConf – JSON, gRPC)

Catalyst 9K
Catalyst 9K Family – Programmability & Automation

- Device Bootstrap and Onboarding
- Configuration Automation through Open Interfaces
- Server Management Tools on x86 Infrastructure

Catalyst 9K Offers Complete DevOps Toolkit
Wrap up…
Catalyst 9K enables the New Era of Networking

X86 Based CPU
Larger Storage

Foundational Components

- Encrypted Traffic Analytics (ETA)
- Resiliency with Patching & GIR
- Programmability & Automation
- Standards Leadership .3bt, .3bz, etc
- Real time Streaming Telemetry
- SD Access
- Trustworthy Systems
- 3rd Party App Hosting
- Fabric Enabled Wireless

Catalyst 9K – Built to see you through Next Decade
Future proofed for the technologies of tomorrow
Cisco Catalyst 9300…

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